AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (original) A circuit that allows a processor forming a part of a microcontroller to change its operating frequency, comprising:

a clock generator generating a plurality of clock signals at a plurality of frequencies;

a first switch receiving the plurality of clock signals and selecting one of the clock signals as an output thereof to be the current clock according to a current speed select signal;

a current speed latch storing the current speed select signal;

a first phase shifter shifting the phase of the current clock to produce a phase shifted current clock;

a second switch receiving the plurality of clock signals and selecting one of the clock signals as an output thereof to be the new clock according to a new speed select signal;

a new speed register storing the new speed select signal; wherein, the new speed select signal is produced by the processor and stored in the new speed register;

a second phase shifter shifting the phase of the new clock to produce a phase shifted new clock; and

logic means, receiving the current clock, the phase shifted current clock, the new clock, the phase shifted new clock and a signal from the processor directing a speed change as inputs thereto, the logic means for producing a signal latching the new speed into the current speed latch at a point in time after the speed change signal when the current clock, phase shifted current clock, the new clock and the phase shifted new clock have the same state.

2. (currently amended) The ~~apparatus~~ circuit according to claim 1, wherein the first and second phase shifter comprise a fixed delay circuit.

3. (currently amended) The ~~apparatus~~ circuit according to claim 1, wherein the first and second phase shifter comprise a fixed delay circuit producing a fixed delay of approximately 21 microseconds.

4. (currently amended) The ~~apparatus~~ circuit according to claim 1, wherein the logic means comprises a logic NOR gate.

5. (currently amended) The ~~apparatus~~ circuit according to claim 1, wherein the speed change signal comprises an I/0 write signal.

6. (currently amended) The ~~apparatus~~ circuit according to claim 1, wherein the plurality of clock signals are generated by dividing a master clock using a series of flip-flops.

7. (original) A circuit that allows a processor forming a part of a microcontroller to change its operating frequency, comprising:

a clock generator generating a plurality of clock signals at a plurality of frequencies;

a first switch receiving the plurality of clock signals and selecting one of the clock signals as an output thereof to be the current clock according to a current speed select signal;

a current speed latch storing the current speed select signal;

a first phase shifter shifting the phase of the current clock to produce a phase shifted current clock;

a second switch receiving the plurality of clock signals and selecting one of the clock signals as an output thereof to be the new clock according to a new speed select signal;

a new speed register storing the new speed select signal;

wherein, the new speed select signal is produced by the processor and stored in the new speed register;

a second phase shifter shifting the phase of the new clock to produce a phase shifted new clock;

logic means, receiving the current clock, the phase shifted current clock, the new clock, the phase shifted new clock and a signal from the processor directing a speed change as inputs thereto; and

the logic means producing a latching signal latching the new speed into the current speed latch at a point in time after the speed change signal when the current clock has the same state as the new clock, and when the phase shifted current clock has the same state as the phase shifted new clock.

8. (currently amended) The ~~apparatus~~ circuit according to claim 7, wherein the first and second phase shifter comprise a fixed delay circuit.

9. (currently amended) The ~~apparatus~~ circuit according to claim 7, wherein the first and second phase shifter comprise a fixed delay circuit producing a fixed delay of approximately 21 microseconds.

10. (currently amended) The ~~apparatus~~ circuit according to claim 7, wherein the logic means comprises a logic NOR gate, and wherein the logic means for producing a signal latching the new speed into the current speed latch at a point in time after the speed change signal when the current clock has the same state as the new clock, the phase shifted current clock and the phase shifted new clock.

11. (currently amended) The ~~apparatus~~ circuit according to claim 7, wherein the logic means comprises a first EXOR gate receiving the current clock and the new clock and a second EXOR gate receiving the phase shifted current clock and the phase shifted new clock, and wherein the first and second EXOR gates have outputs connected to two inputs of a NOR gate with the speed change signal connected to a third input of the NOR gate and with an output of the NOR gate producing the latching signal.

12. (currently amended) The ~~apparatus~~ circuit according to claim 7, wherein the logic means comprises a first NAND gate receiving the current clock and the new clock and a second NAND gate receiving the phase shifted current clock and the phase shifted new clock, and wherein the first and second NAND gates have outputs connected to two inputs of a NOR gate with the speed change signal connected to a third input of the NOR gate and with an output of the NOR gate producing the latching signal.

13. (currently amended) The ~~apparatus~~ circuit according to claim 7, wherein the plurality of clock signals are generated by dividing a master clock using a series of flip-flops.

14. (original) A circuit that allows a processor forming a part of a microcontroller to change its operating frequency, comprising:

a master clock generating a master clock signal;

a clock generator generating a plurality of clock signals from the master

clock signal at a plurality of frequencies by dividing the master clock signal using a plurality of series connected flip flops;

a first switch receiving the plurality of clock signals and selecting one of the clock signals as an output thereof to be the current clock according to a current speed select signal;

a current speed latch storing the current speed select signal,

a first phase shifter shifting the phase of the current clock to produce a phase shifted current clock by delaying the current clock by a fixed delay;

a second switch receiving the plurality of clock signals and selecting one of the clock signals as an output thereof to be the new clock according to a n ew speed select signal;

a new speed register storing the new speed select signal;

wherein, the new speed select signal is produced by the processor and

stored in the new speed register;

a second phase shifter shifting the phase of the new clock to produce a phase shifted new clock by delaying the new clock by a fixed delay; and

a logic NOR gate, receiving as inputs the current clock, the phase shifted current clock, the new clock, the phase shifted new clock and a signal from the processor directing a speed change as inputs thereto, the NOR gate producing a signal latching the new speed into the current speed latch at a point in time when speed change signal, the current clock, phase shifted current clock, the new clock

and,the phase shifted new clock have the same state.

15. (currently amended) The ~~apparatus~~ circuit according to claim 1, wherein the first and second phase shifter comprise a fixed delay circuit producing a fixed delay of approximately 21 microseconds.

16. (original) A method for a processor forming a part of a microcontroller to change its clock frequency, comprising:

at the processor, receiving a clock signal;

determining that the clock frequency is to be changed under program control;

storing a new clock frequency signal in a new speed register;

issuing an I/0 write command indicating that the clock frequency is to change;

in a logic circuit, examining a current clock signal, a new clock signal, a phase shifted current clock signal and a phase shifted new clock signal;

when the current clock signal, the new clock signal, the phase shifted current clock signal and the phase shifted new clock signal reach predetermined states, latching the new clock frequency signal into a current clock speed latch; and

at a switch, receiving an output from the current clock speed latch and

changing a switch setting in response thereto, the switch setting determining the speed of the clock signal

17. (original) The method according to claim 16, further comprising providing the new clock signal and the phase shifted new clock signal to the logic circuit through a switch.

18. (original) The method according to claim 16, wherein the switch receives a plurality of clock signals produced from a master clock signal.

19. (currently amended) The ~~apparatus~~ method according to claim 16, wherein the phase shifted current clock and the phase shifted new clock are delayed versions of the current clock and the new clock respectively, with the delay being a fixed constant delay.

20. (original) The method according to claim 16, wherein the logic circuit examines the current clock signal, the new clock signal, the phase shifted current clock signal and the phase shifted new clock signal to determine that at least the current clock signal has the same state as the new clock signal and the phase shifted current clock signal has the same state as the phase shifted new clock signal.